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EXAMINER	
FRANCIS, MARK P	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/747,598	WU ET AL.	
	Examiner	Art Unit	
	Mark P. Francis	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on December 29, 2003.

2. Claims 1-36 have been examined.

Oath/Declaration

3. The Office acknowledges receipt of a properly signed oath/declaration filed April 26, 2004.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 25-34 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding claim 25,

Applicant defines an apparatus to optimize a program that comprises a cold translator, a hot loop identifier, a gen-translator, and a use-translator all of which can be implemented using software means only (i.e. computer programs per se) that do not necessarily require the use of hardware to perform or execute. Thus, the claim is rejected under 35 U.S.C. 101 as being Non-Statutory.

As a suggestion, Applicant can add the phrase "having a processor" to the preamble to overcome this rejection.

The rejection of the base claim is incorporated into their dependent claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

7. A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-10 and 21-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Mahadevan. (U.S. Pat 5,797,013)

Independent claims

With respect to claims 1 and 35, Mahadevan discloses a machine readable medium storing instructions structured to cause a machine to: cold translate a program from a first language to a second language; (Col 1:17-25, "...reads a source code file and translates it into a high level intermediate representation...")determine a cold execution trip count;(Col 3:20-27, "...the original loop trip count...") insert instructions to calculate a hot execution trip count if the cold execution trip count is less than a predetermined trip count threshold; (Col 8:1-15, "...calculating the lop trip count requires a remainder operation...")

identify a loop in the translated program; (Col 8:1-10, "...the main unrolled loop...")
insert instrumentation into the loop to develop profile data if the hot execution trip count associated with the loop exceeds a predetermined threshold; (Col 10:15-25, "...must not exceed a specific limit...")
and insert a prefetching instruction into the loop if the profile data indicates a load instruction in the loop meets a predefined criteria. (Col 10:23-35, "...If prefetch instructions are being generated...")

With respect to claim 5, Mahadevan discloses a method to optimize a program comprising: cold translating the program from a first instruction set to a second instruction set; (Col 1:17-25, "...reads a source code file and translates it into a high level intermediate representation...")
executing the translated program; (Col 7:52-60, "...shows the output code that is generated ...")
identifying a hot loop in the translated program that meets a first predefined criteria;
gen-translating the hot loop; (Col 10:15-25, "...must not exceed a specific limit...")
and if the hot loop meets a second predefined criteria, use-translating the hot loop. (Col 10:23-35, "...If prefetch instructions are being generated...")

With respect to claim 25, Mahadevan discloses an apparatus to optimize a program(Col 6:54-65, "...effect other optimizations into the longer inner loop code...") comprising: a cold translator to translate the program from a first instruction set to a second instruction

set; (Col 1:17-25, "...reads a source code file and translates it into a high level intermediate representation...")

a hot loop identifier to identify a hot loop in the translated program and to determine if the hot loop should be gen-translated.; (Col 8:6-20, "...if the unroll factor is a power of two...")

a gen-translator to instrument the hot loop with instructions to collect profile information; (Col 8:60-67, "...The value of the two most recent array values must be saved...")

and a use-translator to optimize an instruction associated with the hot loop if the profile information determines that the hot loop should be optimized. (Col 9:15-27, "...optimizer to generate the code...")

Dependent claims

With respect to claim 2, the rejection of claim 1 is incorporated and further, Mahadevan discloses that inserting instrumentation into the loop comprises: finding a load instruction in the loop; (Col 8:53-59, "...loads a[I-2]...")

and inserting a first instruction sequence to record addresses associated with the load instruction. (Col 9:1-18, "...The instruction appears to make an indexed reference to the array A...")

With respect to claim 3, the rejection of claim 2 is incorporated and further, Mahadevan discloses that the first instruction sequence causes the addresses to be recorded in a

buffer associated with the loop, (Col 9:1-18, "...The instruction appears to make an indexed reference to the array A...")

and inserting instrumentation into the loop further comprises: inserting a second instruction sequence into the loop to trigger processing of the addresses in the buffer to determine if the profile data indicates a load instruction in the loop meets a predefined criteria. (Col 10:15-25, "...must not exceed a specific limit...")

With respect to claim 4, the rejection of claim 1 is incorporated and further, Mahadevan discloses that profile data identifies the load instruction as at least one of a single stride load, a multiple stride load, a cross stride load, and a base load of a cross stride load. (Col 8:53-59, "...loads a[I-2]...")

With respect to claim 6, the rejection of claim 5 is incorporated and further, Mahadevan discloses that cold translating the program comprises: identifying a block in a foreign program;(Col 7:50-58, "...in contrast to the code generated...") inserting instructions to update a first counter into an instruction block to determine the number of times the instruction block is executed; and analyzing the first counter to determine if the block is a candidate for optimization. (Col 10:15-25, "...must not exceed a specific limit...")

With respect to claim 7, the rejection of claim 5 is incorporated and further, Mahadevan discloses that gen-translating and use-translating the program each comprises

translating the first instruction set to an intermediate instruction set(Col 8:60-67, "...The value of the two most recent array values must be saved...")
and translating the intermediate instruction set to the second instruction set. (Col 1:17-25, "...reads a source code file and translates it into a high level intermediate representation...")

With respect to claim 8, the rejection of claim 7 is incorporated and further, Mahadevan discloses that the intermediate instruction set comprises an instruction set different than the first instruction set and different than the second instruction set. (Col 1:17-25, "...reads a source code file and translates it into a high level intermediate representation...")

With respect to claim 9, the rejection of claim 5 is incorporated and further, Mahadevan discloses that identifying the hot loop in the translated program comprises conditioning a loop by a least common specialization operation. (Col 8:53-59, "...loads a[I-2]...")

With respect to claim 10, the rejection of claim 9 is incorporated and further, Mahadevan discloses that the least common specialization operation comprises: identifying a block of instructions that is a least common denominator block with other loops; (Col 10:30-37, "...an unroll factor...")
rotating the loop such that the least common denominator block is a head of the loop. (Col 8:60-67, "...the value of the two most recent array values...")

With respect to claim 21, the rejection of claim 5 is incorporated and further, Mahadevan discloses that use-translating comprises: analyzing the profile information; (Col 10:15-35, "...To determine the unroll factor...")
and inserting a prefetching instruction for the load instruction. (Col 6:54-67, "...insert prefetches and effect other optimizations...")

With respect to claim 22, the rejection of claim 21 is incorporated and further, Mahadevan discloses further comprising eliminating redundant prefetched loads. (Col 6:1-5, "...local redundant load elimination..")

With respect to claim 23, the rejection of claim 21 is incorporated and further, Mahadevan discloses that analyzing the profile information comprises determining if the load instruction is at least one of: a single stride load, a multiple stride load, a cross stride load; and a base load. (Col 6:54-67, "...the memory stride...")

With respect to claim 24, the rejection of claim 5 is incorporated and further, Mahadevan discloses further comprising linking the use-translated hot loop into the native program. (Col 1:17-25, "...reads a source code file and translates it into a high level intermediate representation...")

With respect to claim 26, the rejection of claim 25 is incorporated and further, Mahadevan discloses that the hot loop identifier identifies a loop as a hot loop by: counting a number of times an instruction block associated with the loop is executed; determining an average number of times the loop is executed; (Col 10:15-25, "...must not exceed a specific limit...")
and comparing the average number of times the loop is executed to a predetermined threshold. (Col 10:15-25, "...must not exceed a specific limit...")

With respect to claim 27, the rejection of claim 25 is incorporated and further, Mahadevan discloses that the hot loop identifier identifies a hot loop in the translated program by conditioning a loop by a least common specialization operation. (Col 6:54-67, "...insert prefetches and effect other optimizations...")

With respect to claim 28, the rejection of claim 27 is incorporated and further, Mahadevan discloses that the least common specialization operation comprises:

identifying a block of instructions that is a least common denominator block with other loops; (Col 10:5-15, "...compiling loops that range from single instruction inner loops...") rotating the loop such that the least common denominator block is a head of the loop. (Col 9:3-11, "...that suggests that an array access...")

With respect to claim 29, the rejection of claim 25 is incorporated and further, Mahadevan discloses that the gen-translator and the use-translator each translates the program from the first instruction set to an intermediate instruction set and from the intermediate instruction set to the second instruction set. (Col 1:17-25, "...reads a source code file and translates it into a high level intermediate representation...")

With respect to claim 30, the rejection of claim 25 is incorporated and further, Mahadevan discloses that the gen-translator comprises:
a load instruction identifier to identify a load instruction within the hot loop and having at least one predetermined characteristic; (Col 10:15-25, "...must not exceed a specific limit...")
a profiler to insert profiling instructions into the hot loop if the load instruction identifier identifies a load instruction within the hot loop having the at least one predetermined characteristic. (Col 10:27-40, "...If the trip count is constant known...")

With respect to claim 31, the rejection of claim 30 is incorporated and further, Mahadevan discloses that the profiler collects stride information for the load instruction.

(Col 6:55-60, "...also the memory stride...")

With respect to claim 32, the rejection of claim 25 is incorporated and further, Mahadevan discloses that the use-translator comprises: a profile analyzer(e.g. See Fig 14, element 1301) to determine a load instruction type for the load instruction based on the profile data; (Col 10:27-40, "...If the trip count is constant known...")
an optimizer to insert a prefetch instruction into the loop for the load instruction; (Col 10:23-35, "...If prefetch instructions are being generated...")
and a code linker to couple the hot loop to the program. (Col 10:27-40, "...If the trip count is constant known...")

With respect to claim 33, the rejection of claim 32 is incorporated and further, Mahadevan discloses that the optimizer determines an address to be prefetched based on the load instruction type. (Col 8:50-067, "...when the same statement loads...")

With respect to claims 34 and 36, the rejection of claim 32 and 35 are incorporated respectively and further, Mahadevan discloses that the load instruction type comprises at least one of: a single stride load, a multiple stride load, a cross stride load, and a base load of a cross stride load. (Col 6:54-65, "...the memory stride...")

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahadevan (U.S. Pat 5797013) in view of Granston.(U.S. PGPUB 2003/0140334)

With respect to claim 11, the rejection of claims 5 is incorporated and further,

Mahadevan does not disclose that identifying the hot loop in the translated program comprises: using at least one of a cold execution trip count to determine the average number of times the hot loop is executed during cold execution or a hot execution trip count to determine the number of times the hot loop is executed.

Granston discloses that identifying the hot loop in the translated program comprises: using at least one of a cold execution trip count to determine the average number of times the hot loop is executed during cold execution(Col 7:0100, "...to decide if a trip count is less than two...") or a hot execution trip count to determine the number of times the hot loop is executed in an analogous system for the purpose of providing additional information to the compiler that identifies an issue that prevented the compiler from

making a particular optimization due to not enough information. (Mahadevan:Col 1:0008)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to include a cold execution trip count to determine the average number of hot loop execution to Mahadevan's invention using the teachings of Granston.

The modification would have been obvious because one of ordinary skill in the art would have been motivated to send reminder messages to provide additional information to the compiler that identifies an issue that prevented the compiler from making a particular optimization due to not enough information. (Mahadevan:Col 1:0008)

With respect to claim 12, Granston discloses that the cold trip count comprises instructions to determine the frequency a loop entry block is taken and the frequency the loop back edge is taken. (Col 5:0067-0068, "...one for the case where the trip count is above a certain value...")

With respect to claim 13, Granston discloses that the cold trip count comprises instructions that the hot loop is gen-translated if the hot loop contains a load instruction and a value of at least one of a hot trip count and a cold trip count is greater than a predetermined threshold. (Col 5:0067-0068, "...one for the case where the trip count is above a certain value...")

With respect to claim 14, Granston discloses that the hot loop is only gen-translated if the load instruction does not access data in a stack or have a loop invariant load address. (Col 7:0100-0101, "...to decide if a trip count...")

With respect to claim 15, Granston discloses that the hot loop is optimized by a normal hot translation if the cold trip count is less than the predetermined threshold. (Col 7:0100-0101, "...to decide if a trip count...")

With respect to claim 16, the rejection of claim 5 is incorporated and further,

Mahadevan does not disclose that gen-translating comprises: identifying a load instruction within the hot loop; inserting a profiling instruction in association with the load instruction; inserting a profiling control instruction in a loop entry block of the loop to control the number of times the load instruction is profiled; executing the profiling instruction to profile the load instruction; and executing the profiling control instruction to determining if the load has been profiled more than a predetermined number of times.

Granston discloses that gen-translating comprises: identifying a load instruction within the hot loop; (Col 3:0053-0055, "...user loads a saved profile...")

inserting a profiling instruction in association with the load instruction;(Col 4:0066, "...or load a profile dataset...")

inserting a profiling control instruction in a loop entry block of the loop to control the number of times the load instruction is profiled; (Col 5:0068-0069, "...The loop identifier...to collect run time loop profile information...")

executing the profiling instruction to profile the load instruction; (Col 5:0068-0069, "...to collect run time loop profile information...")

and executing the profiling control instruction to determining if the load has been profiled more than a predetermined number of times(Col 5:0067, "...This extra loop is referred ...") in an analogous system for the purpose of providing additional information to the compiler that identifies an issue that prevented the compiler from making a particular optimization due to not enough information. (Mahadevan:Col 1:0008)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to insert a profiling instruction in association with a load instruction to Mahadevan's invention using the teachings of Granston.

The modification would have been obvious because one of ordinary skill in the art would have been motivated to send reminder messages to provide additional information to the compiler that identifies an issue that prevented the compiler from making a particular optimization due to not enough information. (Mahadevan:Col 1:0008)

With respect to claim 17, the rejection of claim 16 is incorporated and further, Granston discloses that the profiling instruction comprises an instruction to assign the load instruction a unique identification number and an instruction to collect profiling information. (Col 5:0068-0069, "...The unique identifiers provided by the profile server...")

With respect to claim 18, the rejection of claim 17 is incorporated and further, Granston discloses that the unique identification number is stored with a data address of the load instruction. (Col 5:0068-0069, "...The unique identifiers provided by the profile server...")

With respect to claim 19, the rejection of claim 16 is incorporated and further, Granston discloses that the profiling information comprises stride information. (Col 5:0069, "...The dataset identifier...")

With respect to claim 20, the rejection of claim 16 is incorporated and further, Granston discloses that the profiling control instruction comprises a counter to determine how many times the load instruction has been profiled. (Col 5:0068, "...record the loop identifier...")

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark P. Francis whose telephone number is (571)272-7956. The examiner can normally be reached on Mon-Fri 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T.An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark P. Francis

Patent Examiner

Art Unit 2193

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